Abstract

A design and verification aide that can be used to produce BZ codes under static or dynamic process, voltage, temperature and external reference resistor (PVT and R) conditions for impedance controlled buffers or any other application using BZ codes. The simulation technique follows that of a flash ADC, and effectively replaces an awkward state-machine BZ controller with a subcircuit consisting of 5 BZREFN's, 5 BZREFP's, 10 HSPICE behavioral comparators, and the BZVREF. The resulting N- and P-codes may be adjusted by a parameterized dither count with minimum and maximum code values enforced by the model, and the comparators can be modified to model offset voltage.